



Effect of Via Pitch on the Extrusion Behavior of Cu-filled TSV

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Abstract: In this study, the extrusion behavior of Cu fill material in a through-Si-via (TSV) subjected to thermal loading was investigated. The Cu filling of the TSV was accomplished using pulse periodic reverse (PPR) electroplating. To study the extrusion, TSVs of varying via pitch were filled with Cu by electroplating. Defect-free Cu filling of the TSV was obtained at a Cathodic Current Density (CCD) of -5 mA/cm^2 . The Cu-filled TSVs were subjected to annealing at $450 \text{ }^\circ\text{C}$ and the extrusion heights were measured. Microstructural characterizations were performed by scanning electron microscopy (SEM) and atomic force microscopy (AFM). The experimental results were also validated using finite element analysis (FEA). The results indicated that as the distance between via holes, i.e., pitch, decreased from 40 to $20 \text{ }\mu\text{m}$, the extrusion heights were found to increase. In other words, the extrusion height increases due to the mutual influence between vias when the spacing of the vias is reduced. The simulated extrusion heights of the Cu-filled TSVs were in good agreement with the experimental results. The FEA simulation results also indicated an overall increasing tendency of extrusion heights when via pitch decreased.

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Keywords: extrusion, through-silicon-via, electroplating, finite element method, thermal expansion coefficient

1. INTRODUCTION

The rapid development of microelectronic packaging and mobile device markets has produced a growing demand for miniaturized, multi-functional and lightweight smartphones, smartwatches, notebooks and related electronic gadgets [1,2]. Moore's law states that the amount of data that can be stored in a microchip will double every 18 months [3,4], and this is reflected in the tremendous efforts being made to increase chip density. However, there is a practical limit to the data density per chip. To deal with this limitation, in the last decade TSV technology has been proposed as a potential technology solution [5-8]. TSV is a next-generation 3D chip packaging technique in which a through-hole structure called a via is fabricated in the silicon die or chip. In this design, chips are stacked

vertically to several tens of microns in thickness. The through holes are filled with a conductive material like copper for inter-connection between the stacked chips [9-11]. Products based on TSV technology such as DDR3 stacked memory, logic 3D SiP/SoC, and MEMS/sensors are currently emerging, and processing technologies to support the commercialization of TSV-related products are being continuously researched.

However, the TSV technology has some remaining challenges. At higher temperature, delamination of wafer and the Cu fill in the via are serious reliability issues which needs to be controlled [12-14]. At wafer thicknesses of less than $100 \text{ }\mu\text{m}$, bending of the Cu conductor and wafer may occur during 3D stacking. This can result from differences in the coefficient of thermal expansion (CTE) of the Cu fill and surrounding Si die, which can skew the entire circuit board. Cu extrusion from the via in TSV also inevitably occurs when fabrication is performed above $350 \text{ }^\circ\text{C}$, such as in the back end of line (BEOL)

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process [15-18]. This Cu extrusion can change the wiring of the electronic component or stress the device.

Accordingly, efforts are being made to suppress such Cu extrusion. Several methods are being examined to avoid extrusion, like using pre-chemical mechanical polishing (CMP) during the BEOL process or installing devices in a stress-free location (keep away zone, KAZ) based on the wafer stress distribution [12]. Tsai *et al.* added the pre-CMP process at 350 °C and successfully limited Cu extrusion to about 50 nm at 400 °C. However, additional extrusion occurred in a subsequent Cu line capping layer deposition stage [14]. Other approaches for extrusion minimization include alloying (Cu-Ni, Cu-W) or the use of nanomaterials like CNT and polymers in Cu [19-22]. However, alloying requires a number of organic additives like complexing agents that may create an unstable plating bath and induce carbon deposits [23,24]. The dispersion of CNT in the Cu is rather tedious job and great attention is needed with polymer filling, which may degrade over time. Most of these works have concentrated on either the Cu fill or study of the extrusion kinetics with temperature [25-28]. At present, there is limited research on the via pitch and its effect on the Cu extrusion. To address this issue, we have experimentally investigated Cu extrusion behavior depending on the via pitch interval, and conducted simulation with finite element analysis (FEA) techniques.

2. EXPERIMENTAL PROCEDURE

2.1 Cu electroplating of TSV

A 6 inch (152.4 mm) wafer containing several vias was cut into a $5 \times 5 \text{ mm}^2$ section using a diamond saw to be filled with Cu by electroplating. A complete wafer prepared by this process with various via pitches is shown in Fig. 1(a,b). The electrolyte for the TSV Cu fill process was composed of organic additives including an accelerator, inhibitor and leveler. The plating cell

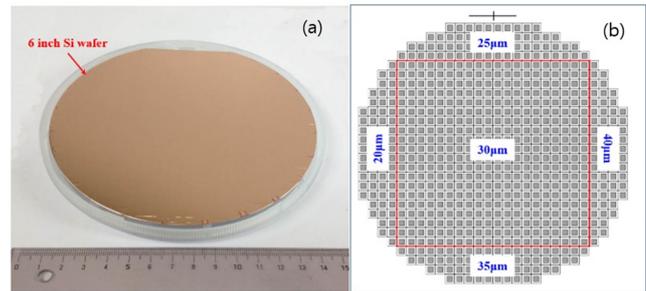


Fig. 1. (a) Fabricated 6 inch Si wafer and (b) pitch difference.

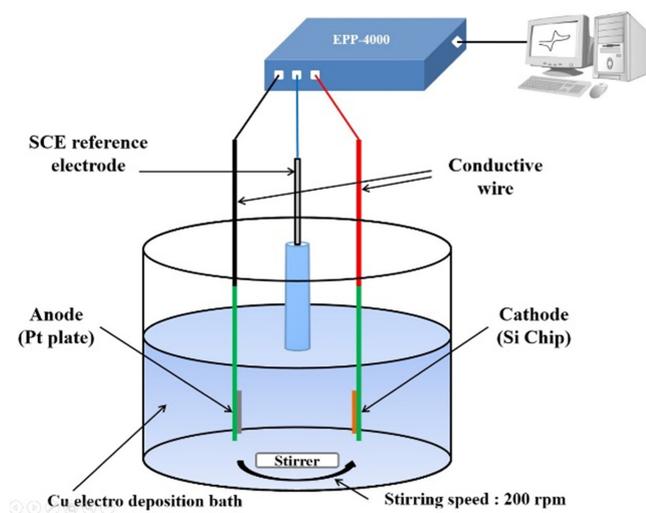


Fig. 2. The three electrode system plating cell.

was composed of an anode (platinum sheet, $10 \times 10 \times 0.3 \text{ mm}^3$) and a saturated calomel electrode (SCE) as a reference. The Si wafer was the cathode substrate in the plating cell. The plating solution was stirred at 200 rpm using a 30 mm long stirrer for proper homogenization of the solution. The temperature of the plating solution was maintained at room temperature and the distance between the electrodes was 30 mm. A three electrode system used for the electroplating process, as shown in Fig. 2. The plating was carried out using an electrochemical pulse plater (EPP-4000, Biologic Science Instruments, France) as the current application and control device. In order to have a defect-free and complete Cu fill in the TSV, the applied current was optimized by using a periodic pulse-reverse (PPR) type waveform.

TSVs that were 10 μm of diameter and 20 μm of depth with various via pitches from 20 to 40 μm were filled using the PPR current waveform. Jung *et al.* have proposed the PPR current plating as an alternative for controlling the plating defects created in the TSVs [19-21]. The PPR current waveform involves a cathodic pulse, anodic pulse and a current-off time. The plating takes place during the cathodic pulse, and uneven projections due to over plating at the via corners are minimized in the anodic pulse. The build-up of a high concentration of copper ions during the anodic pulse at the via corners vanishes during the current-off period [20].

In this study, the PPR plating waveform was optimized by varying the cathodic current density (CCD). The anodic current density (ACD) of the PPR current waveform was fixed at 15 mA/cm^2 , and then the plating current density was decreased from -20 to -5 mA/cm^2 .

2.2 Extrusion characterization

To observe the effect of via pitch on Cu extrusion behavior, specimens with pitches of 20, 25, 30, 35 and 40 μm were filled with Cu using optimum plating conditions (CCD: -5 mA/cm^2 , ACD: 15 mA/cm^2). After plating, the top surfaces of the vias were mechanically polished and subjected to annealing in vacuum at 450 $^{\circ}\text{C}$ for 30 min at a heating rate of 5 $^{\circ}\text{C}/\text{min}$. The top-down and cross-section surfaces of the Cu-filled TSVs were further polished using standard metallographic techniques and a diamond suspension, to allow the examination of microstructures. Field emission scanning electron microscopy (FE-SEM, Hitachi-S4300) was used to identify the top-down surface morphology of the Cu-filled TSVs before and after annealing. The extrusion heights were also measured from SEM images using ImageJ software. Atomic force microscopy (AFM, XE-100) was also employed to study how varying pitch affected extrusion in a more quantitative way. Surface topographies of all the vias were obtained by AFM investigation and compared. Further, the extrusion heights were measured and plotted for all

via pitches and compared.

2.3 Analysis of Cu extrusion by FEA

FEA was performed using ANSYS 14.5, a commercial analysis program, in order to predict the stress distribution and extrusion behavior at different via pitches. A blind TSV with an SiO_2 barrier layer thickness of 1 μm and a diameter and depth of 10 and 20 μm , respectively, was modeled. The analytical modeling was performed using a 3D tetrahedral element. A model of the cross-section of the TSV developed for FEA is given in Fig. 3. The number of total elements and nodes used in the analysis are shown in Table 1. To improve the accuracy of the FEA, the SiO_2 insulating layer and Cu portion were densely meshed. For boundary conditions, the bottom of the Si-wafer was confined in the X, Y, and Z directions, while the sidewall was constrained only in the X and Y directions.

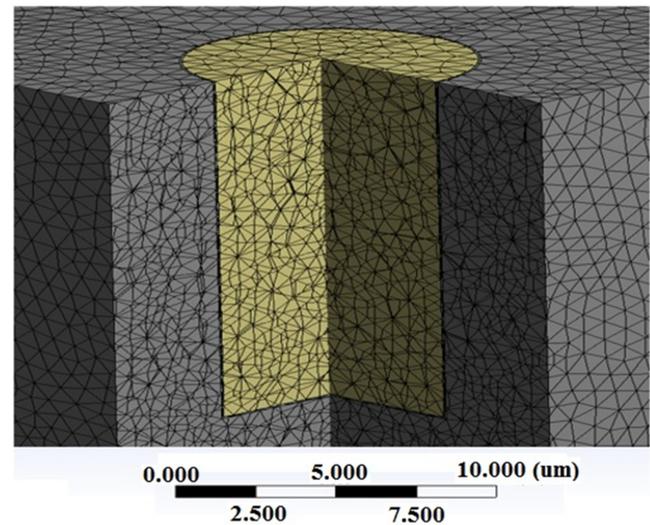


Fig. 3. Quarter symmetric FEM model used for the analysis of the Cu-filled TSV structure.

Table 1. Number of element and node used in modeling.

| | Via pitch (μm) | | | | |
|---------|-----------------------------|---------|---------|---------|---------|
| | 20 | 25 | 30 | 35 | 40 |
| Node | 1014610 | 1549232 | 2202994 | 2725972 | 3538362 |
| Element | 722356 | 1117131 | 1599782 | 1987337 | 2587974 |

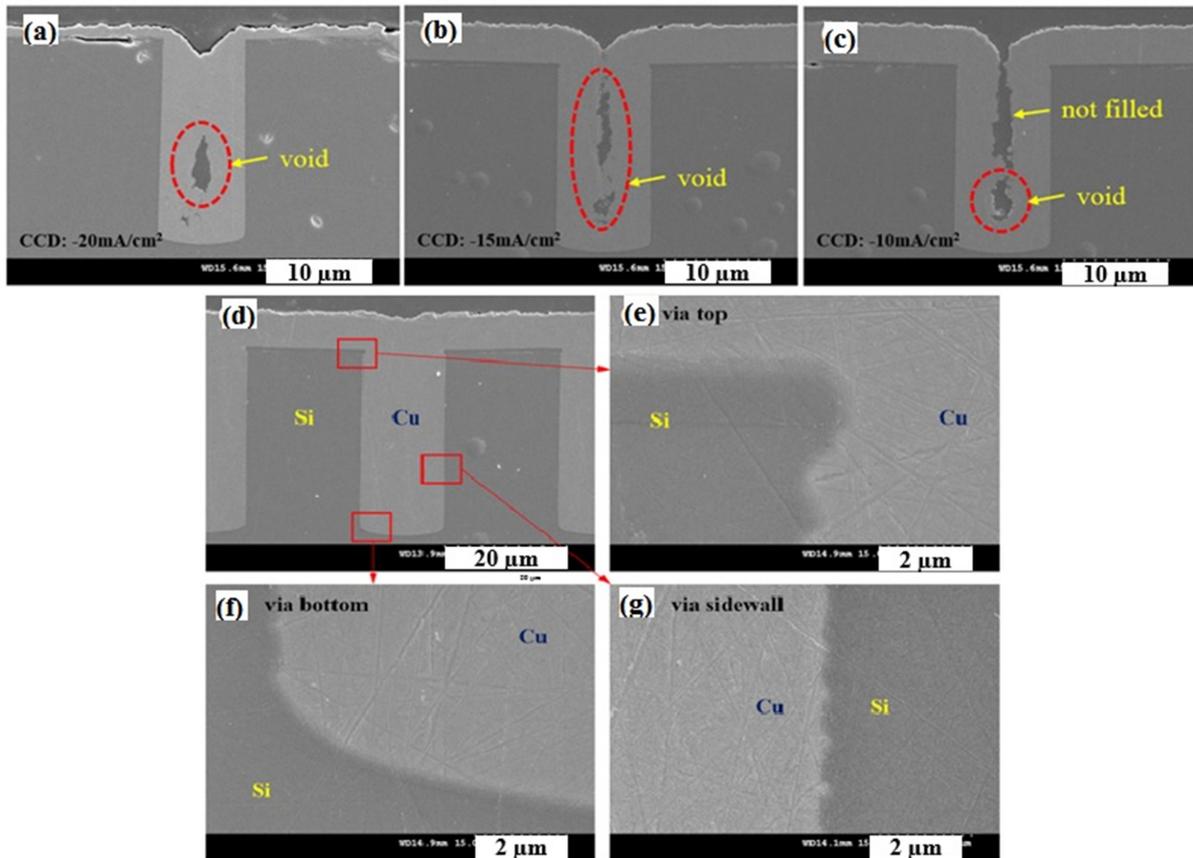


Fig. 4. Cu filling tendency as a function of CCD: (a) -20, (b) -15, (c) -10, and (d) -5 mA/cm² (ACD: 15 mA/cm² for 2 s, current off-time of 10 s); Defect free Cu-filled TSV showing good bonding to the surrounding substrate on (e) top, (f) bottom, and (g) sidewall.

3. RESULTS AND DISCUSSION

3.1 Effect of CCD on Cu filling

Figure 4 shows the cross-sectional SEM images of the Cu-filled TSVs plated at various CCDs from -20 to -5 mA/cm². It is seen that at a CCD of -20 mA/cm², the inlet portion of the via was over-plated and then clogged quickly, creating a big pore (Fig. 4(a)). With a further reduction in CCD to -15 and -10 mA/cm², the pore changed to a seam (Fig. 4(b,c)). This may be due to the high value of CCD. At a higher CCD, the population density of Cu ions is increased, causing an enhanced deposition rate. However, increased CCD may generate progressive hydrogen evolution resulting in the formation of pores and voids.

A high flow rate of Cu ions toward the cathode increases the diffusion of Cu ions drastically and the

via entrance becomes clogged down [19,20]. This result is consistent with other studies where a high CCD increases the deposition rate significantly. A completely filled via without any defects was achieved at a CCD of -5 mA/cm² (Fig. 4(d)). In this case no defects were found, such as peeling in the bonding surface between the via and seed layer on the via top, via sidewall, or via bottom. This can be confirmed from the top, bottom and sidewall interface images observed at high resolution (Fig. 4(e,g)). Therefore, the CCD of -5 mA/cm² for 20 s (at constant ACD of 15 mA/cm² for 2 s, and current off-time of 10 s) was chosen to fill via for further experiments. The total filling time for all the TSVs was around 2 h.

3.2 Extrusion characterization

3.2.1 Scanning electron microscopy

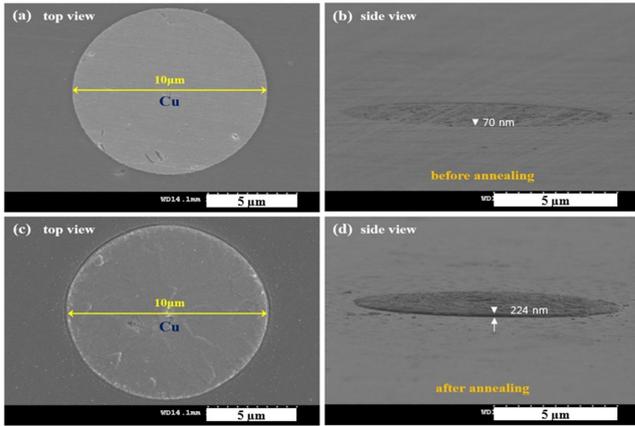


Fig. 5. Top-down and side view surface images of Cu-filled TSVs: (a) top view before annealing, (b) side view before annealing, (c) top view after annealing, and (d) side view after annealing (annealing condition: 30 min at 450°C).

Figure 5(a,b) shows the top down surface images of the Cu-filled TSV before and after annealing. It can be seen that the top down surface of Cu-filled TSV is irregular before annealing. As analyzed by the ImageJ software, the top surface image of the Cu-filled TSV lies 70 nm deeper than the surface of the Si wafer (Fig. 5(b)). This phenomenon is thought to be due to the fact that the Si wafer has a higher hardness, of about 10 GPa, as compared to electrodeposited Cu (≈ 1.4 GPa). As a consequence, Cu is easily polished away during mechanical polishing.

Figure 5(c,d) show the top down surface images of Cu-filled TSV after annealing. The Cu-filled TSV above the Si wafer looks like a step of a definite height, and the slightly extruded shape over the Si wafer was confirmed after annealing. The Cu extrusion heights were different for different via pitch. The extrusion height of the Cu-filled TSV above the Si surface was measured to be ≈ 200 nm. The height of each extrusion was measured five times, and the average value was taken. The extrusion heights results are given in Table 2.

Although all the vias were filled completely before annealing, the extrusion heights at different via pitches were still different. Table 2 shows the extrusion heights of the Cu-filled TSVs before and after annealing at various pitches. It can be seen that the

Table 2. Average Cu extrusion heights at various via pitches

| Via pitch (μm) | Extrusion height (nm) |
|-----------------------------|-----------------------|
| 20 | 199.524 |
| 25 | 193.203 |
| 30 | 183.518 |
| 35 | 180.413 |
| 40 | 178.889 |

extruded heights of the Cu-filled TSVs lie in the range of 178~200 nm after annealing. It was also observed that the extruded heights fall gradually with increasing via pitch. The extrusion process becomes slightly slower, i.e., (≈ 180 and ≈ 179 nm at 35 and 40 μm , respectively). This can be attributed to stress interference between adjacent Si vias when the pitch of the Si vias becomes narrow [31]. To study them in detail quantitatively, the extrusion heights were measured using an AFM technique as discussed in the following sections.

3.2.2 Atomic force microscopy

To produce a more accurate picture of the extrusion tendency at different via pitches, AFM measurements were performed as shown in Fig. 6. It was found that before annealing, the morphology was rather planar, and the features along the Z-axis increased rapidly after annealing. The final extrusion height (h_l) can be defined as Eq. 1,

$$h_l = h_a - h_m \quad (1)$$

where, h_m is the extrusion height before annealing and h_a is the extrusion height after annealing. The AFM images demonstrate that Cu has been extruded out of the via, and the extrusion heights are different for different via pitches. It can be seen that the Cu extrusion heights fall gradually with increasing via pitch up to 35 μm , and the heights become steady thereafter. For example, as the pitch increased from 25 to 35 μm , the extrusion heights decreased in the order of 193.203, 183.518, and 180.413 nm. The extrusion height for $p = 20$ μm was a maximum ≈ 199.524 nm after annealing. As already discussed, this is probably due to the fact that as the pitch increases, extrusion

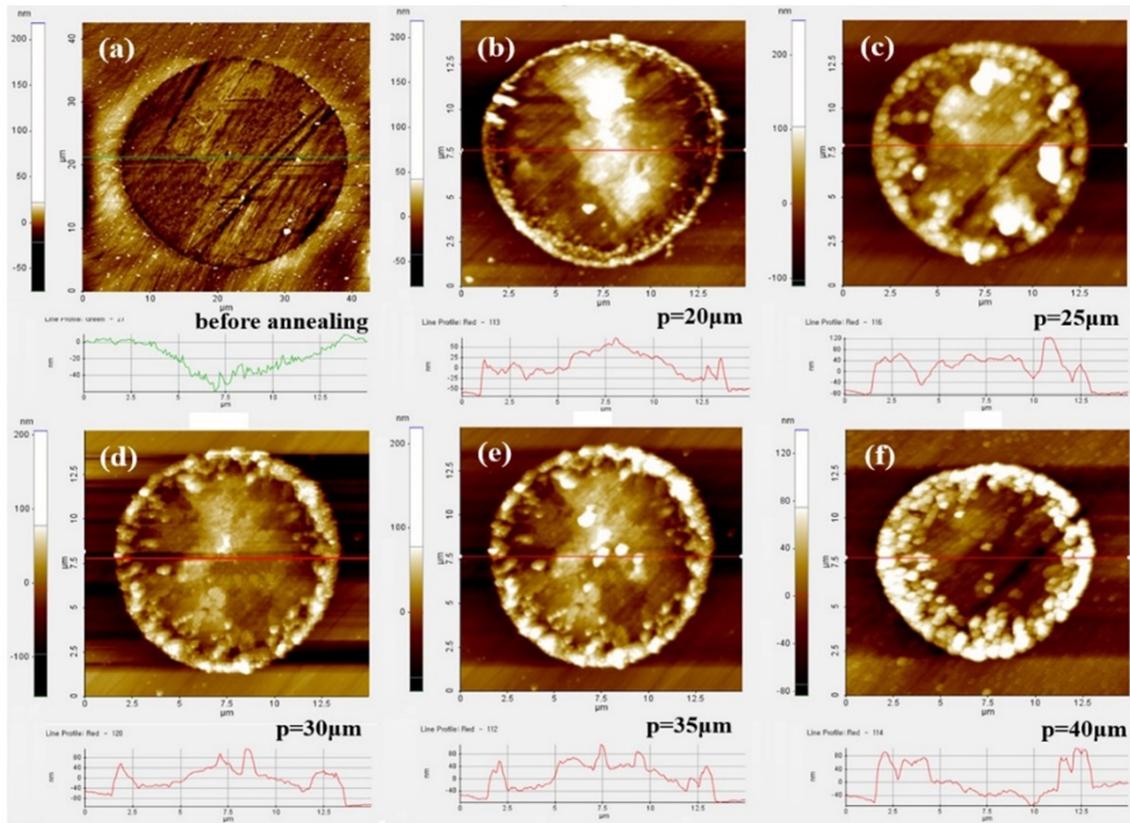


Fig. 6. Cu extrusion height of the vias at different pitch after annealing: (a) as polished, (b) 20, (c) 25, (d) 30, (e) 35, and (f) 40 μm .

is less affected by the stress between adjacent vias. Beyond via pitch $p=35\ \mu\text{m}$, the extrusion height did not change much ($\approx 178.889\ \text{nm}$ at $p=40\ \mu\text{m}$). This observation confirms that there is a via pitch beyond which the extrusion becomes minimum.

As reported in a recent study by Roh *et al.*, the Cu filling extrudes in a vertical direction [19]. After annealing of the Cu-filled TSV, thermal stresses build up due to the CTE mismatch between the Cu filling and Si wafer. When the thermally-induced stress in the Cu-filled TSV exceeds the elastic range of Cu, the Cu deforms plastically, and this leads to Cu extrusion. Since the bottom portion of the via is confined by the Si-wafer filled with Cu, height and stress can be calculated from the partially constrained thermal deformation. In this study, the calculated height obtained in the absence of adjacent vias was $144.7\ \text{nm}$. However, in a real silicon chip, there are several adjacent vias. Therefore, the amount of thermal

deformation must be greater than $144.7\ \text{nm}$, as shown in the result given in Table 2. The Cu extrusion heights at different pitch measured by AFM were also compared using the finite element modeling results in Section 3.3.

3.3 Analysis of Cu extrusion by FEA

The experimentally obtained Cu extrusion heights at various via pitches were modeled using the FEA technique. The model chosen for the TSV was similar in structure to the actual TSV shape. The pitches of the Si vias were set to $p=20, 25, 30, 35,$ and $40\ \mu\text{m}$, respectively. Figure 7 shows the distribution of von-Mises stress seen from the top of the silicon wafer at various via pitches (20, 25, 30, 35, and $40\ \mu\text{m}$). For pitch $p=40\ \mu\text{m}$, the von Mises stress is at least $\approx 1407.2\ \text{MPa}$. As the pitch becomes larger, i.e., $p=25, 30,$ and $35\ \mu\text{m}$, the von-Mises stress gradually increases to $1428.8, 1466.5,$ and $1481.9\ \text{MPa}$, respectively.

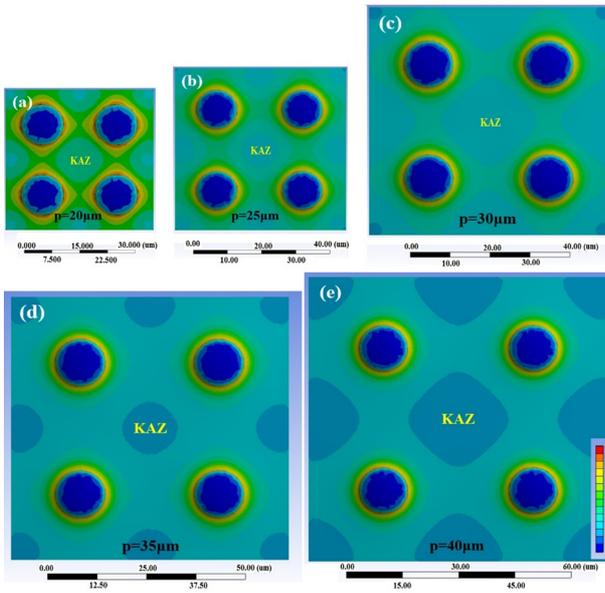


Fig. 7. Von-Mises stress distribution (top view) according to Si via pitch: (a) 20, (b) 25, (c) 30, (d) 35, and (e) 40 μm .

Beyond $p = 35 \mu\text{m}$, there is slight change in the stress value, i.e., 1484.5 MPa (for $p = 40 \mu\text{m}$). It was also observed that irrespective of via pitch, the von-Mises stress was mainly concentrated at the interface between the Cu and the SiO_2 layer. It should be noted that if the von-Mises stress is greater than the yield stress of the filling material (Cu), permanent deformation may occur, causing fracture and delamination of the silicon wafer and Cu.

The increase in stress value with decreasing via pitch can be attributed to the reduced area of the KAZ as shown in Fig. 7. KAZ is a region where stress interference between Si vias does not occur. In other words, when the pitch increases, the KAZ area increases and stress distribution inside the via decreases. However, there is a slight effect of stress distribution inside the via at a pitch $p = 40 \mu\text{m}$ ($\approx 1445.8 \text{ MPa}$). This means a minimum pitch of 35 μm or more is promising for minimizing thermal deformation due to annealing. Athikulwongse *et al.* reported that to reduce the stress interference between TSVs, the KAZ region should be as large as possible when designing the structure of the TSV [32].

From the preceding sections, it is clear that the

von-Mises stresses are higher ($\approx 1400 \text{ MPa}$) compared to the calculated stress ($\approx 939.25 \text{ MPa}$) for a single via (without adjacent vias), with the thermal deformation being 144.7 nm (Table 2). It can be inferred that the stress increases from 939 to 1484 MPa, a 58% increase, when adjacent vias are present. Similarly, the thermal deformation increases from 144.7 to 199.79 nm, showing an increment of 28% in extrusion height. The resultant stress field at a single TSV is the superposition of all the stress fields exerted by the adjacent individual TSVs [31]. Therefore, the stress increases drastically due to the stress interference between adjacent vias when the via pitch is reduced [31].

Figure 8 shows cross-sectional views of the simulated Cu deformations at various pitches. As seen, the von-Mises stress distribution is highly concentrated near the via entrance as well as at the bottom edge near the SiO_2 layer. When the via pitch was increased from 20 to 40 μm , the stress decreased from 1432.2 to 1402.2 MPa near the entrance and from 1302.3 to 1195.7 MPa at the bottom edge, respectively. In is inferred that the stress produced in the Cu-filled TSVs is relaxed when there are fewer vias, meaning there is less probability of Cu extrusion.

The CTE of Cu is about $17 \times 10^{-6} / ^\circ\text{C}$ which is 6 times greater than that of Si ($2.8 \times 10^{-6} / ^\circ\text{C}$) and about 28 times greater than that of the SiO_2 insulating layer ($0.6 \times 10^{-6} / ^\circ\text{C}$). Therefore, the thermal stresses are high enough to deform Cu permanently in the form of an extrusion and leave it deformed even after cooling. The stresses developed in these two regions (the top and bottom corners) were four times greater than the average stresses in the other regions. Moreover, the copper filling is confined in the surrounding of silicon wafer, which has a very high yield stress of 7 GPa. The yield stress of the electroplated Cu varies from 200 to 600 MPa, and is known to be influenced by grain size, temperature as well as the thickness of the plated layer. When the temperature rises during annealing, compressive stresses build up in the radial direction and tensile stress is generated in the axial direction. It is clear that the Cu is constrained along

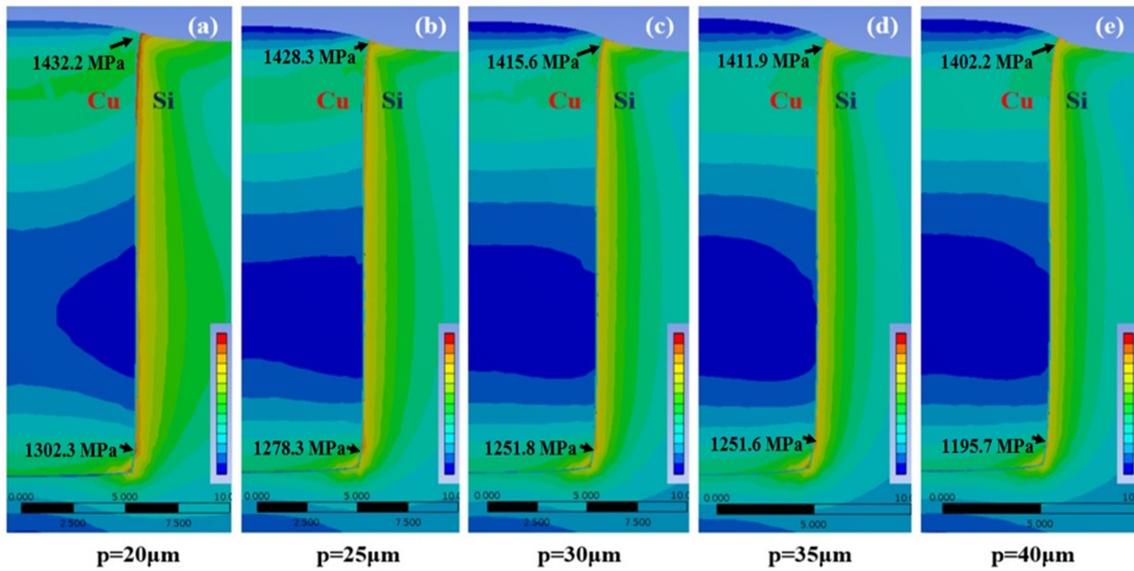


Fig. 8. Von-Mises stress distribution (cross-section view) according to Si via pitch: (a) 20, (b) 25, (c) 30, (d) 35, and (e) 40 μm .

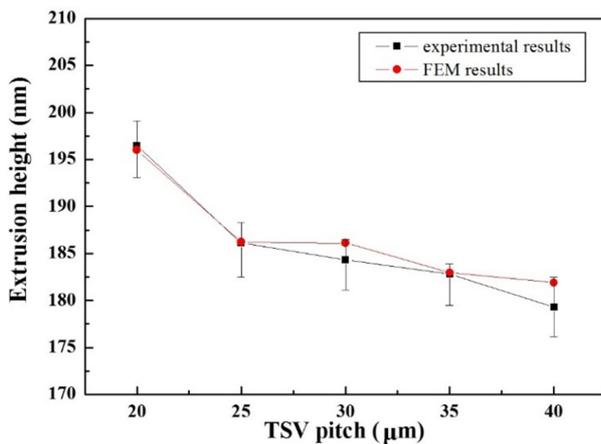


Fig. 9. Extrusion height at different via pitch.

the radial and axial direction of the via as well as at the bottom. Therefore, the plastic deformation of Cu occurs in the vertical direction, causing Cu extrusion on the Si wafer surface [19,22].

Figure 9 shows both the experimental and simulation results for the Cu extrusion heights. It can be observed that the extrusion height at 40 μm pitch is lowest ≈ 181.7 nm. As the pitch increases, $p=20$, 25, 30 and 35 μm , the extrusion height decreases to 199.79, 189.97, 185.13, and 182.87 nm, respectively. The extrusion height becomes steady at and beyond $p=35$ μm . In other words, the effect of via pitch

becomes insignificant when via pitch becomes double the original size. Therefore, a minimum pitch, $p=35$ μm or more is recommended for the extrusion minimization. The results of Cu extrusion by FEA differs slightly, there is a slight variation in extrusion height as compared to experimental measurements. However, the general trend appears the same, suggesting that the Cu extrusion height increases with decreasing TSV pitch.

4. CONCLUSIONS

In this study, changes in stress and the height of Cu extrusions in vias depending on TSV pitch were examined, and the experimental results were compared with the results of finite element analysis. The results are summarized as follows.

1. The electroplated Cu-filled TSVs were defect-free and filled with 100% efficiency when the cathodic current density of the pulse periodic reverse current waveform was lowered from -20 to -5 mA/cm^2 .

2. The extrusion heights of the Cu-filled TSVs decreased rapidly after annealing, (i.e., 199.524, 193.203, 188.518, and 180.413 nm) when the via pitch was increased from 20 to 35 μm , and became stable (≈ 178.889 nm) after further increase in pitch to 40 μm .

The stress and thermal deformation experienced by a

Cu-filled TSV (for a single via when there are no adjacent vias) as calculated by numerical methods were 939.25 MPa and 144.5 nm, respectively. However, when adjacent vias were present, the stress and amount of thermal deformation increased due to stress interference from other vias.

The von Mises stress determined in the finite element analysis was in the order of 1484.5, 1481.9, 1466.5, 1428.7 and 1407.2 MPa as the via pitch increased to 20, 25, 30, 35, and 40 μm , respectively. The extrusion height in the finite element analysis was 199.79 nm at a via pitch of 20 μm , which decreased to 189.97, 185.13, 182.87, and 181.69 nm, respectively as the pitch increased to 25, 30, 35, and 40 μm due to the stress relaxation at higher via pitches.

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